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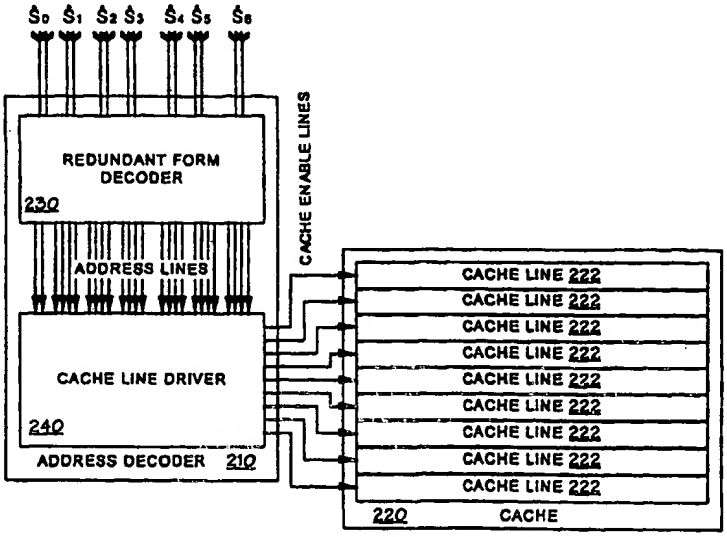

(57) Abstract

A memory system includes a memory (220, 520) having a plurality of memory lines (222, 522) and an address decoder (210, 510) that enables one of the memory lines in response to a redundant form address signal. A redundant form decoder (230, 530) decodes redundant form data into a differential pair of decoded address signals, for each bit position of a memory address, which are applied to a memory line driver (240, 540). One of the two differential pairs carries correct address data. The one address line to be used is determined on a memory line basis, using the address of the memory lines themselves. The redundant form address decoder avoids a completion add that would otherwise be required, yielding very fast access to memory.

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REDUNDANT FORM ADDRESS DECODER FOR CACHE SYSTEM STORING ALIGNED DATA

BACKGROUND

The present invention relates to an address decoder for a memory.

Microprocessors and other integrated circuits store data in memory systems. The memory systems store digital data such as program instructions or variable data. Shown in FIG. 1, a typical memory system 100 includes an address decoder 110, a memory 120 and, optionally, a selection switch 130. The memory 120 is organized into rows, called "memory lines." Each memory line possesses a unique address. When an address is applied to the address decoder 110, the address decoder 110 causes data stored in the associated memory line to be output from the memory system 100.

In certain applications, it may be preferable to retrieve only part of a memory line. For example, a processor may load data into the memory 120 one memory line at a time but may use the loaded data in smaller increments. In this type of application, the selection switch 130 permits a selected portion of a memory line to be output from the memory system 100. An output port of each memory line is coupled to a common bus that is applied to the selection switch. Thus, data from an enabled memory line is provided to the selection switch 130.

The selection switch 130 selects a part of the memory line to be provided from the memory system 100.

To reference a desired portion of data in the form of signals, the address decoder 110 typically receives an address signal that identifies not only a requested memory line but also a portion of the memory line. The memory line is identified by a first part of the address ($Addr_s$-$Addr_n$); the portion of the memory line is identified by a second part of the address ($Addr_0$-$Addr_{s-1}$).

The address decoder 110 is shown in greater detail in FIG. 2. The address decoder 110 is populated by a plurality of AND gates, one per memory line in memory 120. Each AND gate, such as gate 112, receives an input signals for each bit position i that references the memory line (i = s to n). Also for each bit position i, the address signals $Addr_i$ are inverted ($Addr_i$#) so that either the true value of the address bit or its complement may be applied to an AND gate. For any AND gate, the gate is coupled to the one of $Addr_i$ or $Addr_i$# that is a one when the appropriate address signal is applied.

For example, AND gate 112 should enable its memory line when address "0000" is applied to the address decoder. In response to "0000," $Addr_i = 0$ for all i. However, $Addr_i$#=1 for all i. Therefore AND gate 112 receives input signals from $Addr_0$#, $Addr_1$#, $Addr_2$#, etc. Similarly, AND gate 114 should enable its memory line when address "0001" is applied to the address decoder. Therefore, $Addr_i$# is applied to AND gate 114 for all $i \neq 0$. For address "0001," $Addr_0$=1 and is applied to the AND gate 114 instead of $Addr_0$#. Each AND gate is coupled to the address lines in accordance with the address to which the AND gate should be responsive.

It is a goal of memory systems to retrieve requested data as quickly as possible. Any delays that occur between the time that an address is posted and the time that the requested data is available for use are undesirable. At times, however, address data may be posted as one or more arithmetic operations. The arithmetic

operations must be performed before an address may be applied to the address decoder 110. Traditional arithmetic operations are slow; they impose the undesired delay to data retrieval operations.

A traditional adder is shown in FIG. 3. There, four bit inputs X and Y are added together to obtain a four-bit sum S and a single bit carry C_{out}. The adder includes an internal carry chain that propagates between every bit position in the adder. A carry from a first bit position may affect the value of the sum at a second bit position (S_2). A carry from the second bit position may affect the value of the sum at a third bit position (S_3). The carry chain continues through to the most significant bit. Because the carries affect the value of the sum result, true results cannot be output from the adder until the carry chain has traversed the entire length of the adder.

When several arithmetic operations are performed sequentially, carry chains must be completed for each operation. Sequential arithmetic operations on address data cause memory operations to be very slow.

Accordingly, there is a need in the art for a memory system that provides for fast retrieval of requested data when data is subject to arithmetic operations.

"Redundant form" adders are known to be faster than traditional adders. An example of a three input redundant form adder is shown in FIG. 4. There, the adder generates a multi-bit sum, labeled "Ö," from inputs W, X and Y. Each "bit position" in the resulting sum (such as $Ö_2$) actually is represented by two bits. The redundant form adder does not possess the internal carry chain found in traditional adders. Accordingly, redundant form arithmetic operations are very fast relative to traditional arithmetic operations. To obtain a traditional, non-redundant result, the two bits at each bit position must be added together by a traditional adder. For example, the two bits of each sum position Öi output by the redundant form adder may be input to the traditional adder of FIG. 3 to obtain a non-redundant result.

Traditional memory cannot operate on address data that is input in redundant form. No known memory system performs address decoding on address data in redundant form.

SUMMARY

Embodiments of the present invention provide a memory system that retrieves data based upon redundant form address data. The memory system includes a memory having a plurality of memory lines and an address decoder that enables one of the memory lines in response to a redundant form address signal.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a known memory system.

FIG. 2 is a block diagram of a known address decoder for a memory system.

FIG. 3 is a block diagram of a traditional adder circuit.

FIG. 4 is a block diagram of a known redundant form adder circuit.

FIG. 5 is a block diagram of a memory system constructed in accordance with a first embodiment of the present invention.

FIG. 6 is a block diagram of a redundant form decoder circuit constructed in accordance with an embodiment of the present invention.

FIG. 7 is a block diagram of a redundant form decoder constructed in accordance with an embodiment of the present invention.

FIG. 8 is a block diagram of a combinatorial stage of a redundant form address decoder constructed in accordance with an embodiment of the present invention.

FIG. 9 is a block diagram of a memory system constructed in accordance with

a second embodiment of the present invention.

FIG. 10 is a block diagram of a combinatorial logic stage constructed in accordance with a second embodiment of the present invention.

FIG. 11 is a block diagram illustrating how addition of two non-redundant values to obtain a result in redundant form employing no addition.

DETAILED DESCRIPTION

An embodiment of the present invention provides a memory system that retrieves data based upon address information input signals in redundant form. When arithmetic operations are performed on address data signals, data retrieval from memory systems is made faster than data retrieval from traditional systems.

FIG. 5 illustrates a memory system 200 constructed in accordance with a first embodiment of the present invention. The memory system 200 includes an address decoder 210 and a memory 220. The address decoder 210 receives address data signals in redundant form; that is, two bits per "bit position" $Ö_i$. For notational purposes, the two bits of $Ö_i$ are labeled A_i and B_i respectively. Based on the value of the redundant form address data signals, the address decoder 210 accesses a selected memory line 222 in the memory 220. The memory 220 outputs signals data from the selected memory line 222.

The address decoder 210 may be a two-stage decoder in this embodiment. The first stage 230 comprises a redundant form decoder in which the redundant form address data signals are decoded into address signal lines in the embodiment. For all bit positions i ($i \neq 0$), the redundant form decoder 230 generates four address signals, labeled Z_{ia}, Z_{ib}, Z_{ic} and Z_{id}, in differential pairs ($Z_{ia}=Z_{ib}\#$, $Z_{ic}=Z_{id}\#$). The redundant form decoder 230 is populated by a number of redundant form decoding circuits (not shown). The second stage comprises a memory line driver 240 in which the address decoder 210 generates memory line enable signals based upon data signals on the

address lines.

FIG. 6 illustrates a redundant form decoder circuit 300 for bit position $\ddot{O}_i$ ($i \neq 0$) constructed in accordance with an embodiment of the present invention. The decoder circuit 300 generates address signals Z_{ia}, Z_{ib}, Z_{ic} and Z_{id} based upon the values of $\ddot{O}_i$ (A_i, B_i) and $\ddot{O}_{i-1}$ (A_{i-1} and B_{i-1}). Values A_i, B_i, A_{i-1} and B_{i-1} are input to the decoder 300 on input ports 302, 304, 306 and 308 respectively. Address signals Z_{ia}, Z_{ib}, Z_{ic} and Z_{id} are output from the decoder 300 on output ports 310, 312, 314 and 316 respectively.

A_i and B_i are input signals to a first XOR gate 320. XOR gate 320 generates an output signal on line 322. Line 322 is input to a pair of XOR gates 324 and 326. XOR gate 324 generates the first differential pair of address signals Z_{ia} and Z_{ib}. XOR gate 326 generates the second differential pair of address signals Z_{ic} and Z_{id}.

A_{i-1} and B_{i-1} are input to an AND gate 328 and to an OR gate 334. AND gate 328 generates an output signal on line 332 which is input to XOR gate 324. The OR gate 334 generates an output signals on line 338 which is input to XOR gate 326.

The redundant form decoder circuit 300 resembles a traditional adder to a great degree. Line 322 represents a non-redundant sum that would be obtained by adding A_i to B_i. Lines 332 and 338 represent carries from position i-1 under appropriate circumstances:

The signal on line 332 represents the carry from position i-1 when $S_{i-1}=1$ (as described later).

The signal on line 338 represents the carry from position i-1 when $S_{i-1}=0$ (as described later).

Thus, either Z_{ia} or Z_{ic} represents the non-redundant sum bit S_i. Identification of the one address line that carries the correct value of S_i is determined based on additional information. This is discussed in connection with FIG. 8 below.

A traditional adder, however, employees an internal carry chain that propagates through every bit position in the addition in this embodiment. The redundant form decoder circuit 300 does not include any carry in from position i-2 in this embodiment.

The redundant form decoder circuit 300 may be but one stage of a multi-bit decoder. The gates shown in FIG. 6 may be shared with other stages to form a complete multi-bit decoder. For example, additional gates 340 and 342 (shown in phantom) illustrate gates that would be provided to couple input signals A_i and B_i to the i+1 position decoder. They correspond to gates 328 and 334 in the i^{th} position decoder. Gate 330 (also in phantom) may be used in an i-1 position decoder.

FIG. 7 illustrates a redundant form decoder circuit 400 constructed in accordance with an embodiment of the present invention. The decoder circuit 400 is suitable for use with redundant form bit $\ddot{O}_0$. Again, for notational purposes, the two bits of $\ddot{O}_0$ are represented as A_0 and B_0 respectively. They are input to the decoder circuit 400 at input terminals 402 and 404. The decoder circuit 400 generates a single differential pair of address lines Z_{0a} and Z_{0b} on output terminals 406 and 408.

A_0 and B_0 are input to an XOR gate 410. XOR gate 410 generates an output signal on line 412. A carry in C_{in}, if provided for bit position 0, is input at input terminal 416. A second XOR gate 414 receives input signals from line 412 and terminal 416. The second XOR gate 416 generates Z_{0a} and Z_{0b} on output terminals 406 and 408. If no carry in C_{in} is provided, the second XOR gate 414 may be omitted. Z_{0a} and Z_{0b} may be generated directly from the first XOR gate 410.

FIG. 8 illustrates a circuit diagram of a memory line driver 250 of the address decoder 210 (FIG. 5) constructed in accordance with an embodiment of the present invention. The memory line driver 250 is populated by a number of AND gates 252-256. Each AND gate (such as gate 252) is provided in association with one of the memory lines in the memory 220 (FIG. 4). Each AND gate 252 receives one of the

address lines Z_{ia}-Z_{id} (i=1 to n) from the redundant form decoder 230 as an input. Each AND gate 252 also receives one of the pair of address lines Z_{0a}-Z_{0b} for bit position i=0. In response to an address input signal to the memory system in redundant form, one of the memory lines should be enabled.

As noted with respect to the redundant form decoder 300 of FIG. 6, one of address lines Z_{ia} and Z_{ic} carry the correct signal value of non-redundant S_i. The correct signal value could be determined from an internal carry chain typical to conventional adders (sometimes called the "completion add"). However, improved performance maybe obtained by omitting the internal carry chain.

In this embodiment each AND gate 252, 254, etc. maps to a memory line having a unique address R. The address may be used as an additional piece of information to identify which of Z_{ia} or Z_{ic} carries the correct value of non-redundant S_i. Specifically, the non-redundant value of the address R at bit position i-1 (R_{i-1}) is taken to be the value of the non-redundant sum S_{i-1} (R_{i-1}=S_{i-1}). This assumption is justified because, if it were not true, then some other input signal to the AND gate would be zero during the address decoding process. The AND gate might not drive its associated memory line in such a circumstance. In other words, the AND gate will function when the completion add would have generated a S_{i-1} that agrees with the address bit R_{i-1}. When the input signals values A_i, B_i, A_{i-1} and B_{i-1} are known and the non-redundant sum S_{i-1} is "known" to be R_{i-1}, the non-redundant value S_i may be calculated.

Table 1 below illustrates the values of S_i and the values Z_{ia}-Z_{id} output from the redundant form decoding circuit 300 for all possible permutations of A_i, B_i, A_{i-1}, B_{i-1} and S_{i-1}. The table is sorted first by S_{i-1}, then by S_i. As the table illustrates, when S_{i-1} is 0, Z_{ic}=S_i. When S_{i-1} is 1, Z_{ia}=S_i.

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	B_i	A_{i-1}	B_{i-1}	S_{i-1}	S_i	Z_{ia}	Z_{ib}	Z_{ic}	Z_{id}
0	0	0	0	0	0	0	1	0	1
0	1	0	1	0	0	1	0	0	1
0	1	1	0	0	0	1	0	0	1
0	1	1	1	0	0	0	1	0	1
1	0	0	1	0	0	1	0	0	1
1	0	1	0	0	0	1	0	0	1
1	0	1	1	0	0	1	0	0	1
1	1	0	0	0	0	0	1	0	1
0	0	0	1	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
0	0	1	1	0	1	1	0	1	0
0	1	0	0	0	1	1	0	1	0
1	0	0	0	0	1	1	0	1	0
1	0	1	0	0	1	0	1	1	0
1	1	1	0	0	1	0	1	1	0
1	1	1	1	0	1	1	0	1	0

A_i	B_i	A_{i-1}	B_{i-1}	S_{i-1}	S_i	Z_{ia}	Z_{ib}	Z_{ic}	Z_{id}
0	0	0	0	1	0	0	1	0	1
0	0	0	1	1	0	0	1	1	0
0	0	1	0	1	0	0	1	1	0
0	1	1	1	1	0	0	1	0	1
1	0	1	1	1	0	0	1	0	1
1	1	0	0	1	0	0	1	0	1
1	1	0	1	1	0	0	1	1	0
1	1	1	0	1	0	0	1	1	0
0	0	1	1	1	1	1	0	1	0
0	1	0	0	1	1	1	0	1	0
0	1	0	1	1	1	1	0	0	1
0	1	1	0	1	1	1	0	0	1
1	0	0	0	1	1	1	0	1	0
1	0	0	1	1	1	1	0	0	1
1	0	1	0	1	1	1	0	0	1
1	1	1	1	1	1	1	0	1	0

Table 1

Of course, an AND gate is responsive only when it receives input signals that are 1. However, sometimes the correct value of S_i is 0 (when R_i=0). If S_i were input to the AND gate, it would not function even though the selected value of S_i is correct. Thus, when the correct value of S_i is selected but S_i=0, S_i is inverted and input to the AND gate. Because Z_{ib}=Z_{ia}# and Z_{id}=Z_{ic}#, they are used as input signals when S_i=0.

Thus, for each bit position i (i≠0), an AND gate is coupled to one of the four address lines Z_{ia}-Z_{id} based upon the non-redundant values of the address bits R_i, R_{i-1}. Table 2 demonstrates how the connections are made:

Value of Address for AND Gate		Selected Address Line
R_i	R_{i-1}	
0	0	Z_{id}
0	1	Z_{ib}
1	0	Z_{ic}
1	1	Z_{ia}

Table 2

In FIG. 8 the AND gates 252-255 illustrate couplings made in accordance with this principle for i=1.

As described with reference to FIG. 5, bit position i=0 is used to address a memory line. For each AND gate related to an address R terminating in 0 (R_0=0), the AND gate receives an input from line Z_{0b} in this embodiment. For each AND gate related to an address terminating in 1 (R_0=1), the AND gate receives an input signals from line Z_{0a} in this embodiment.

When the least significant bit of the redundant form input data signals is used in the address of the memory lines 222, in this embodiment of the present invention may be used with no completion add. However, a completion add may be employed when the least significant bit of the redundant form data does not address the memory. For example, if redundant form input data extends from $Ö_0$-$Ö_n$ but bits $Ö_3$-$Ö_n$ address the memory lines, a completion add may be employed for redundant form bits $Ö_0$-$Ö_3$.

FIG. 9 illustrates a memory system 500 constructed in accordance with a second embodiment of the present invention. In the second embodiment, aligned data signals may be read out of a memory based on redundant form address data signals. The memory system 500, like the system 200 of FIG. 5, includes an address decoder 510 and a memory 520. The address decoder 510 comprises a two-stage decoder including a redundant form decoder 530 and a memory line driver 540. The memory system 500 also includes a selection switch 550.

In the second embodiment, of the redundant form address bits $Ö_0$-$Ö_{s+n}$ subject to arithmetic preprocessing, only a portion of the bits $Ö_s$-$Ö_{s+n}$ is employed to address individual memory lines. The remaining bits, $Ö_0$-$Ö_{s-1}$ represent data signals within a memory line.

The memory system 500 of FIG. 9 reads out "aligned data." Aligned data comprises data signals that are contained within a predefined block in a memory line. Each memory line 522 is divided into a plurality of blocks. Two blocks are shown in FIG. 9: High order blocks and low order blocks. Within a memory line, the blocks are identified by address data S_{s-1} at position s-1. In this embodiment, requested data

may not cross a boundary between blocks.

The redundant form decoder 530 is populated by multiple stages of the redundant form decoder circuit 300 of FIG. 6. The redundant form decoder circuit 300 applied for use in decoding all redundant sum bits $\ddot{O}_i$ for i = s to s+n.

FIG. 10 illustrates a memory line driver 540 of the address decoder 510 constructed in accordance with an embodiment of the present invention. The memory line driver is populated by a number of AND gates each associated with a block of each memory line. Thus, in the memory line driver 540 of FIG. 9 there are twice as many AND gates as there are memory lines. Where each memory line is assigned an address R composed of bits R_s to R_{s+n}, the blocks within each memory line are addressed by lower order bits R_{s-1} to R_{s-m}. In the two-block example of FIG. 9, bit R_{s-1} addresses the blocks within a memory line.

For each bit position i (i from s to s+n), each AND gate receives as an input signal of the address lines Z_{ia}, Z_{ib}, Z_{ic} or Z_{id} generated by the redundant form decoder stage 540. Identification of the one address line Z_{ia}-Z_{id} to which an AND is coupled is determined by the AND gates' address bit R_i and R_{i-1} according to the principle outlined in Table 2 above.

In the memory line driver 540 of FIG. 10, two AND gates 541, 542 are responsive to a predetermined redundant form address. A first AND gate 541 selects a low order block. The selected low order block is addressed correctly when S_{s-1}=0. A second AND gate 542 selects a high order block. The selected high order block is addressed correctly when S_{s-1}=1. The selection switch 550 (FIG. 9) determines which selected block of data is routed out of the memory system 500.

The requested block of data is selected by selection switch 550 based on non-redundant S_{s-1}. Initially, S_{s-1} is not known. To obtain S_{s-1}, it may be desirable to perform a traditional add of the redundant form address data Ö for bit positions 0 through s-1. When a non-redundant value of S_{s-1} is obtained, it is applied to the

selection switch 550 to select the correct block of data. The block selected by the selection switch 550 is the one whose decoding AND gate is known to have received a correct input signal.

Although a completion carry addition may be performed in the embodiment of FIG. 8, this embodiment still achieves improved performance over the systems of the prior art. The carry chain propagates only through bits 0 through s-1, not through the entire length of the address (0 though s+n). Thus, the carry chain is reduced.

The time employed to perform the short address add may be justified also due to operational characteristics of a memory memory. Traditionally, memory memories are somewhat slow to output data from a memory line once the memory line is enabled. There is an inherent latency in the time that data is available to a selection switch once a memory line is enabled. Thus, performing a traditional add on the short run of address data, from bits 0 to s-1, does not impair significantly the speed at which data may be retrieved from the memory.

Alternatively, control signals input to the selection switch 550 may be generated using the logic of FIG. 8. The selection switch itself may be controlled by redundant form logic.

The discussion of the redundant form address data provided above has assumed that one or a series of redundant form arithmetic operations are performed on address data before resultant address data is input to an address decoder. In a special case, arithmetic processing may be omitted from a memory operation. When a memory operation causes a single addition of two non-redundant addresses to be performed, the memory operation may be omitted. Instead, the two non-redundant addresses may be input directly to the address decoding.

As shown in FIG. 11, a redundant form addition of two non-redundant numbers, generates a redundant form sum Ö, where:

$$\ddot{O}_i = A_i, B_i, \text{ for all } i.$$

Thus, this embodiment of the present invention provides for zero delay decoding of address data in a single addition implementation.

This embodiment of the present invention provides an address decoder that decodes address data in redundant form. The address decoder permits arithmetic operations to be made on address data at very high speed and, therefore, reduces latency of memory operations that rely on those arithmetic operations. Because the address decoder omits the internal carry chain common to traditional adders, it provides dramatic performance benefits over conventional memory operations involving arithmetic operations.

Several embodiments of the present invention are specifically illustrated and described herein. However, it will be appreciated that modifications and variations of the present invention are covered by the above teachings and within the purview of the appended claims without departing from the spirit and intended scope of the invention.

WE CLAIM:

1. A memory system, comprising:

an address decoder receiving on an input redundant form address data signals and including memory enable lines as output ports, and

a memory populated by a plurality of memory line entries, at least one entry coupled to at least one of the memory enable lines.

2. The memory system of claim 1, wherein the address decoder comprises:

a redundant form decoder stage, adapted to receive the redundant form address data signals and to generate decoded address signals on address lines, and

a memory line driver stage, coupled to the address lines and including the memory enable lines as output ports.

3. The memory system of claim 2, wherein:

at least one memory enable line is associated with a predetermined address of a predetermined width,

the address decoder comprising a multi-stage decoder included a stage associated with at least one bit position in the address.

4. The memory system of claim 3, wherein at least one decoder circuit stage is adapted to generate decoded address signals based upon the redundant form address data at the associated bit position and the next lower bit position.

5. The memory system of claim 3, wherein at least one decoder circuit stage is adapted generate a pair of decoded address signals for the associated bit position.

6. The memory system of claim 5, wherein the memory line driver stage includes an AND gate associated with one of the addresses, the AND gate adapted to receive one of the pair of decoded address signals as an input signal, the one decoded address

signal determined by the value of the one address at the bit position of the decoder circuit stage and the next lower bit position

7. The memory system of claim 2, wherein two memory enable lines are provided for each memory line entry, one for a first half of the memory line entry, the other for a second half of the memory line entry.

8. The memory system of claim 7, further comprising a selection switch coupled to each half of the memory line entries, said selection switch capable of being controlled by the address decoder.

9. The memory system of claim 2, wherein the memory line driver stage comprises a plurality of AND gates, each AND gate associated with a unique address in the memory, wherein an AND gate receives predetermined ones of the address lines in accordance with its unique address.

10. A redundant form address decoder, comprising:

a redundant form decoder, adapted to receive address data in redundant form and generating decoded address signals on address lines, and

a memory line driver, coupled to the address lines and adapted to generate an output signal on memory enable lines.

11. The redundant form address decoder of claim 10,

wherein a memory enable line is associated with an address of a predetermined width, and

the redundant form decoder comprises redundant form decoding circuits, one provided in association with a bit position of the address.

12. The redundant form address decoder of claim 11, wherein at least one redundant form decoding circuit adapted to generate two differential pairs of address

lines in response to redundant form address data input at its associated bit position and the adjacent lower bit position.

13. The redundant form address decoder of claim 11, wherein the redundant form decoding circuit associated with the least significant bit of the address comprises a one bit adder.

14. The redundant form address decoder of claim 10, wherein the memory line driver comprises a plurality of AND gates, an AND gate associated with an address of a predetermined width and selectively coupled to the address lines in accordance with its address.

15. The redundant form address decoder of claim 14, wherein, for at least one bit position of the address, the address lines comprise two differential pairs of address lines.

16. A memory system, comprising:

a memory having a plurality of memory line entries, a memory line entry organized into a high order half and a low order half, a high order half and low order half coupled to a respective memory line drive line,

an address decoder, receiving address data signals in redundant form, the address decoder having as outputs the memory line drive lines, and

a selection switch coupled to the halves of the memory line entry.

17. The memory system of claim 16, wherein the selection switch receives a control signal as an input signal, the control signal being output from the address decoder.

18. The memory system of claim 17, wherein:

the control signal comprises a multi-bit control signal identifying one of a

plurality of blocks of data within a half of a memory line, and

responsive to the multi-bit control signal, the selection switch outputs a selected block from the memory system.

19. The memory system of claim 16, where the address decoder comprises:

a multi-bit decoder that decodes the redundant form address data into decoded address lines, and

a memory line driver stage coupled to the decoded address lines and including as outputs the memory line drive lines.

20. The memory system of claim 19, wherein at least one stage of the multi-bit decoder is associated with a predetermined bit position of the redundant form address data and the stage receives as input signals the redundant form address data at the bit position and an adjacent lower bit position.

21. A method of controlling a memory system, comprising:

receiving on an input redundant form address data signals,

generating a memory enable signal based on the redundant form address data signals,

applying the memory enable signal to a memory, and

reading data from the memory based upon the memory enable signal.

22. The method of claim 21, wherein

the receiving step includes generating decoded address signals based on the redundant form address signals, and

the generating step includes generating the memory enable signal from the decoded address signals.

23. The method of claim 22, wherein the redundant form address signals are

organized as a plurality of multi-bit bit positions and at least one decoded address signal is generated based upon the value of the redundant form address data at an associated bit position and a next lower bit position.

24. The method of claim 23, wherein the decoded address signals for at least one bit position are generated as a differential pair of decoded address signals.

25. The method of claim 24,

wherein the memory includes memory entries, each associated with a memory enable signal and with a memory address, and

the generating step includes enabling a memory enable signal based upon a predetermined combination of decoded address signals.

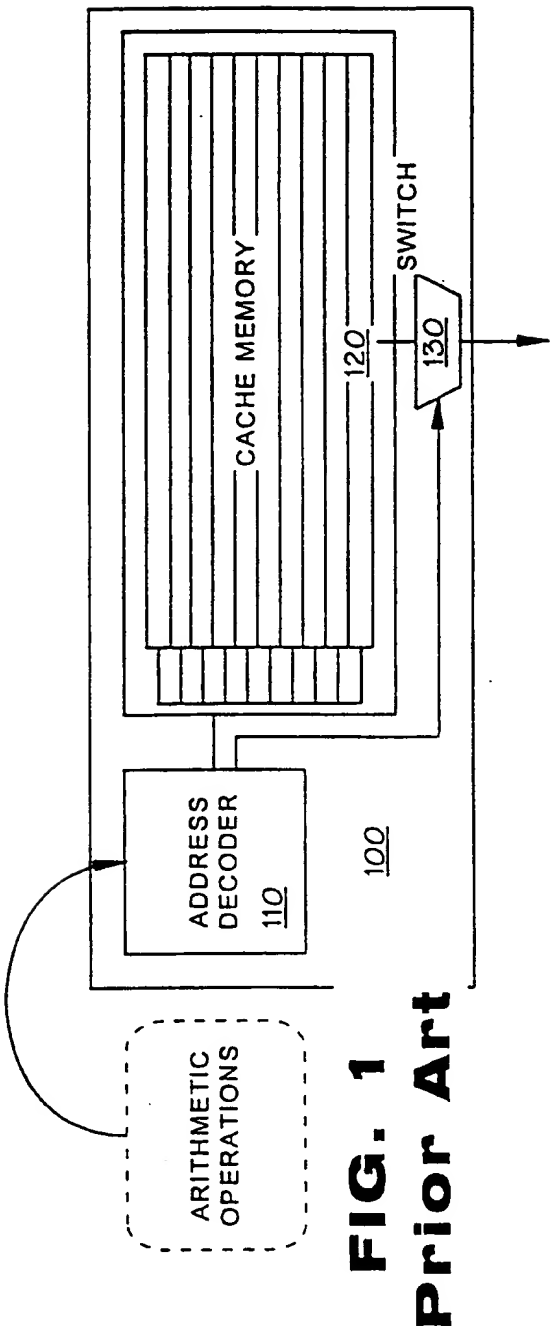


FIG. 1
Prior Art

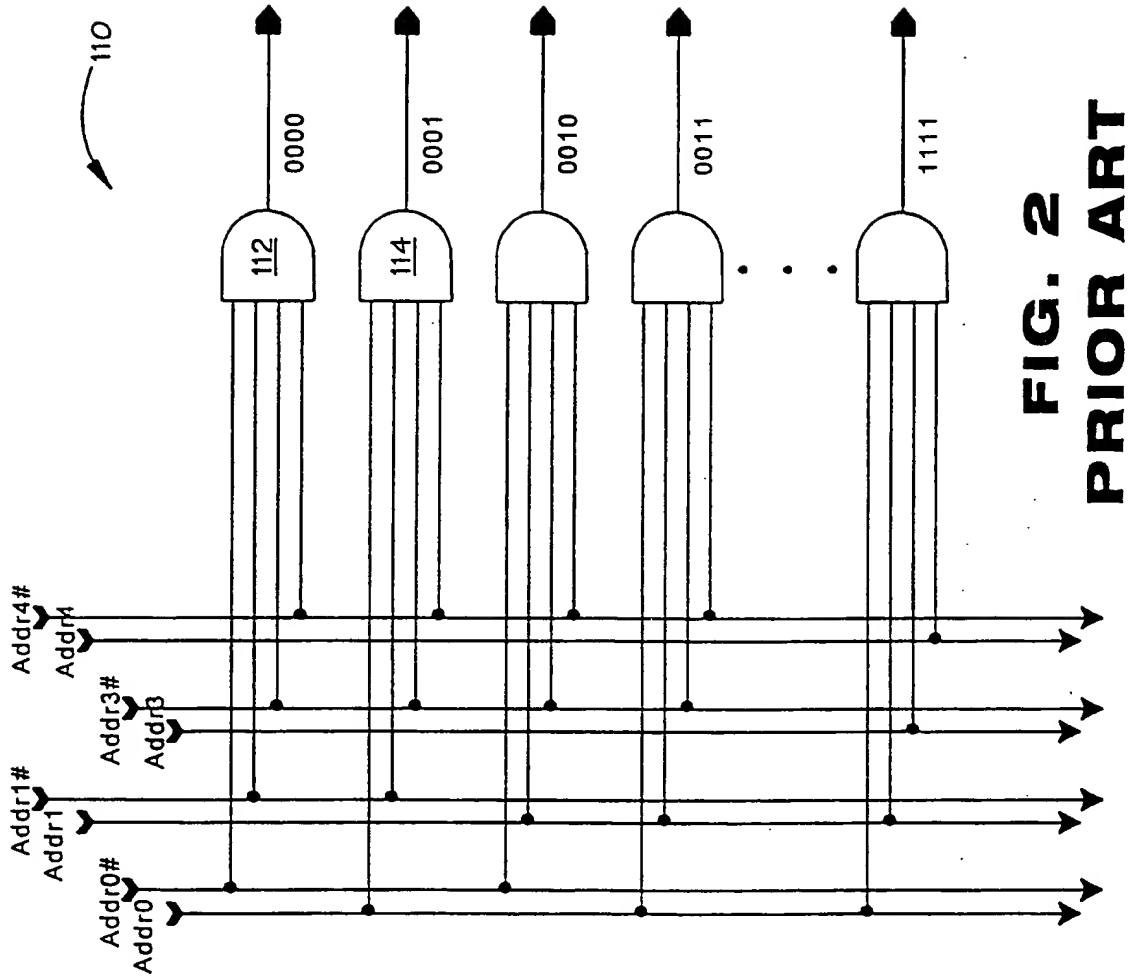


FIG. 2
PRIOR ART

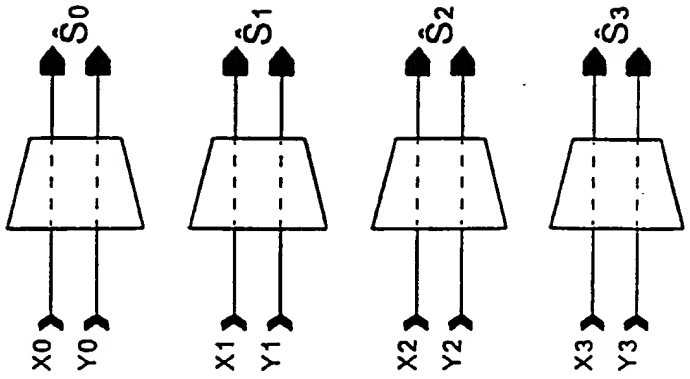


FIG. 11

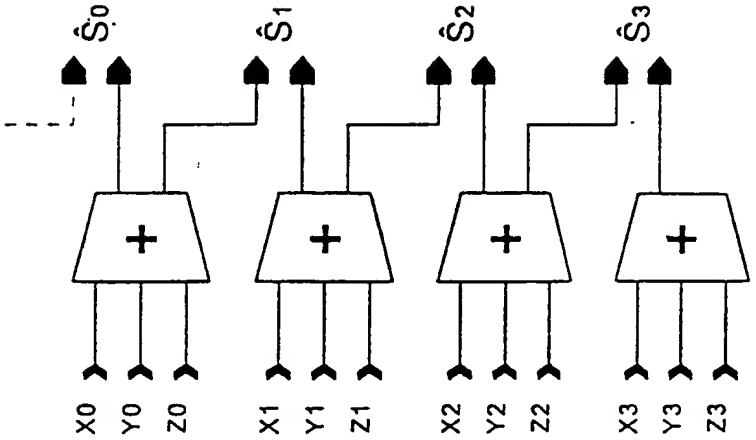


FIG. 4
Prior Art

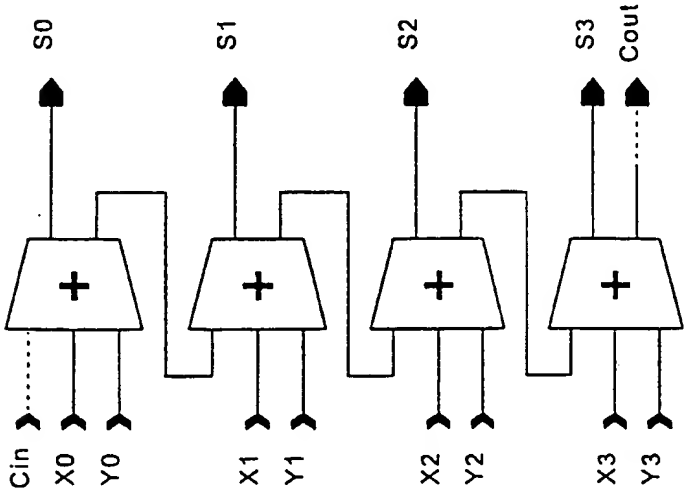


FIG. 3
Prior Art

FIG. 5

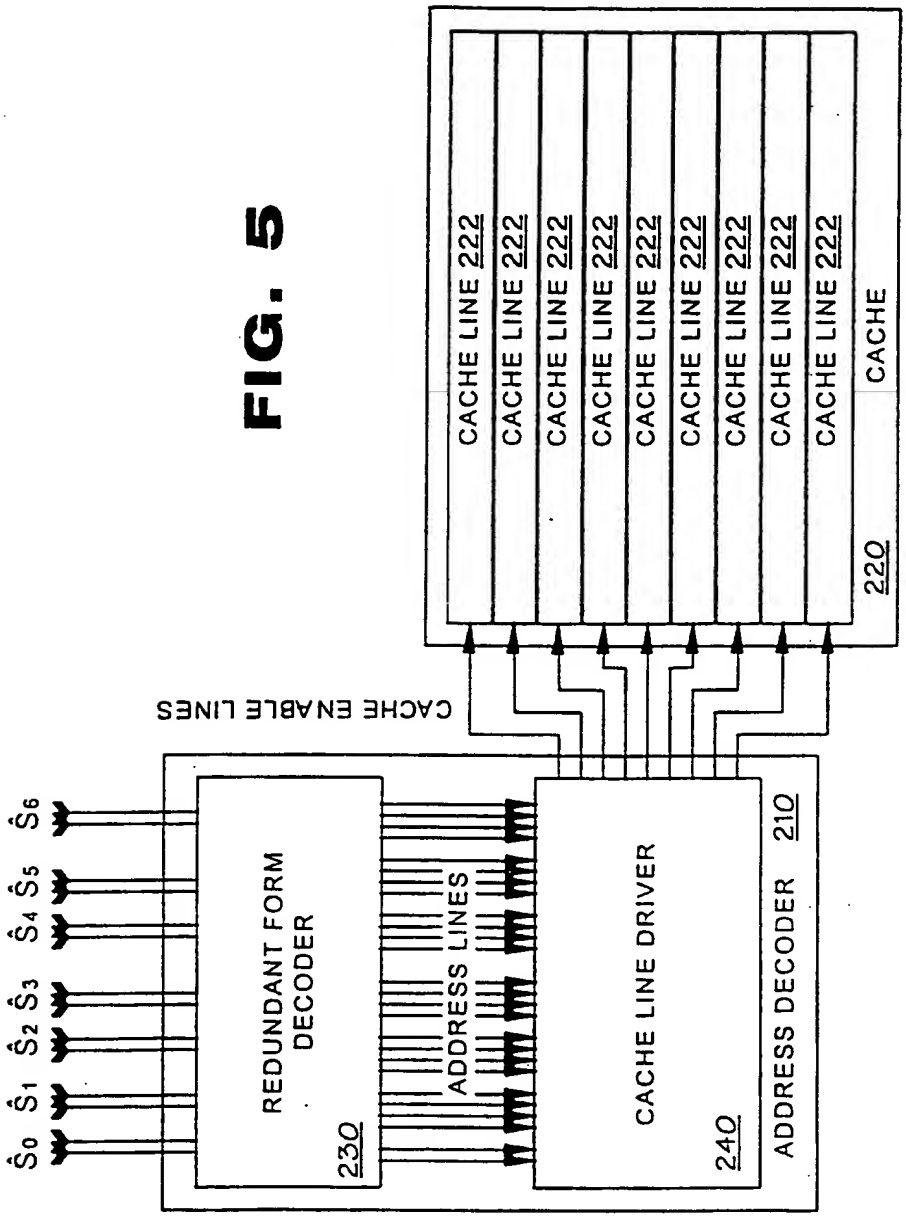

CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE LINE 222
CACHE
220
CACHE ENABLE LINES
$\hat{S}_0$ $\hat{S}_1$ $\hat{S}_2$ $\hat{S}_3$ $\hat{S}_4$ $\hat{S}_5$ $\hat{S}_6$
REDUNDANT FORM DECODER
230
ADDRESS LINES
CACHE LINE DRIVER
240
ADDRESS DECODER
210

FIG. 6

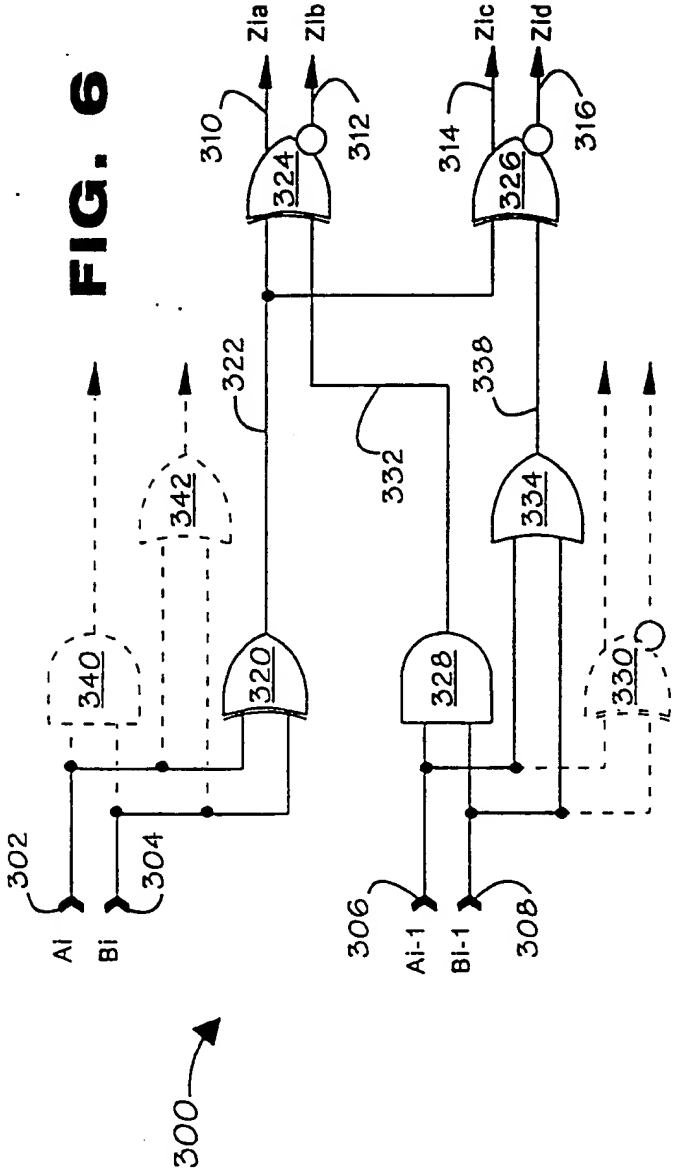

Z1a
Z1b
Z1c
Z1d
310
312
314
316
324
326
322
332
338
334
342
340
320
328
330
302
304
306
308
Ai
Bi
Ai-1
Bi-1
300

FIG. 7

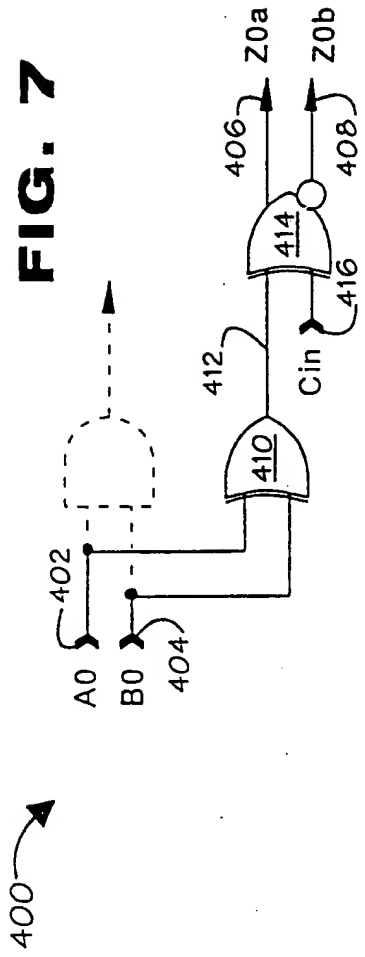

Z0a
Z0b
406
408
414
416
412
Cin
410
402
404
A0
B0
400

FIG. 8

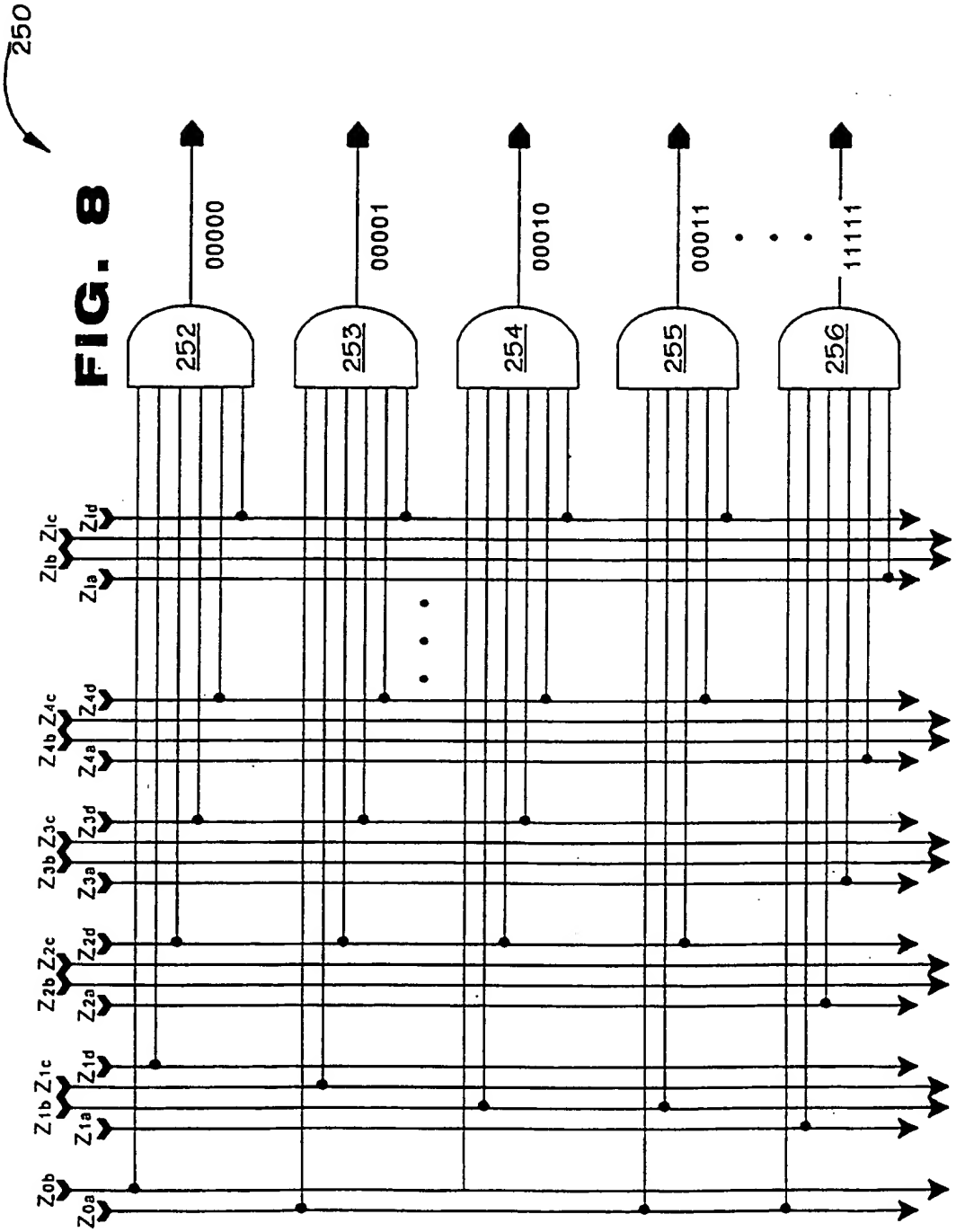

250
252
253
254
255
256
00000
00001
00010
00011
11111
Z1b Z1c Z1d
Z1a
Z4b Z4c Z4d
Z4a
Z3b Z3c Z3d
Z3a
Z2b Z2c Z2d
Z2a
Z1b Z1c Z1d
Z1a
Z0b
Z0a

FIG. 9

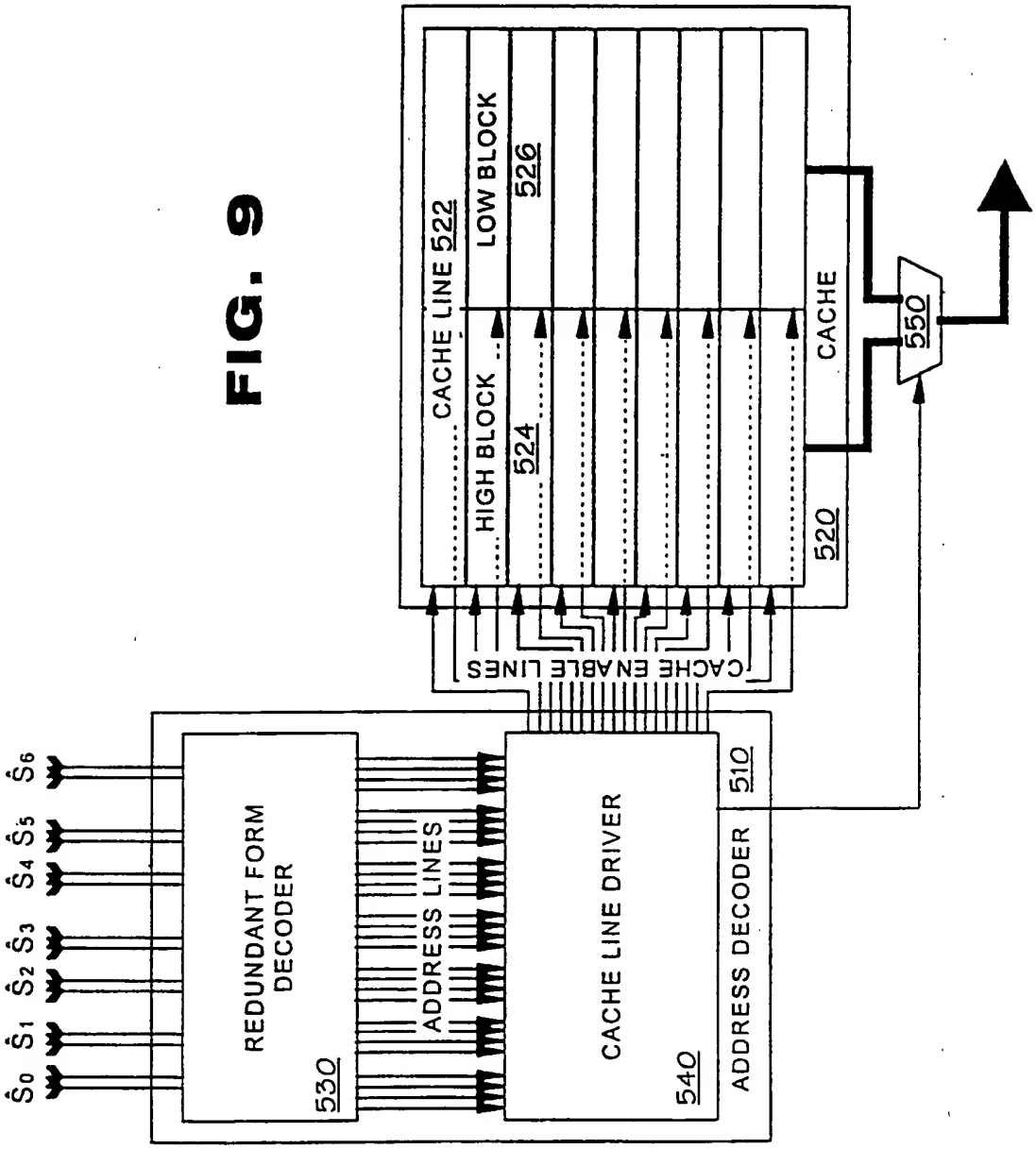
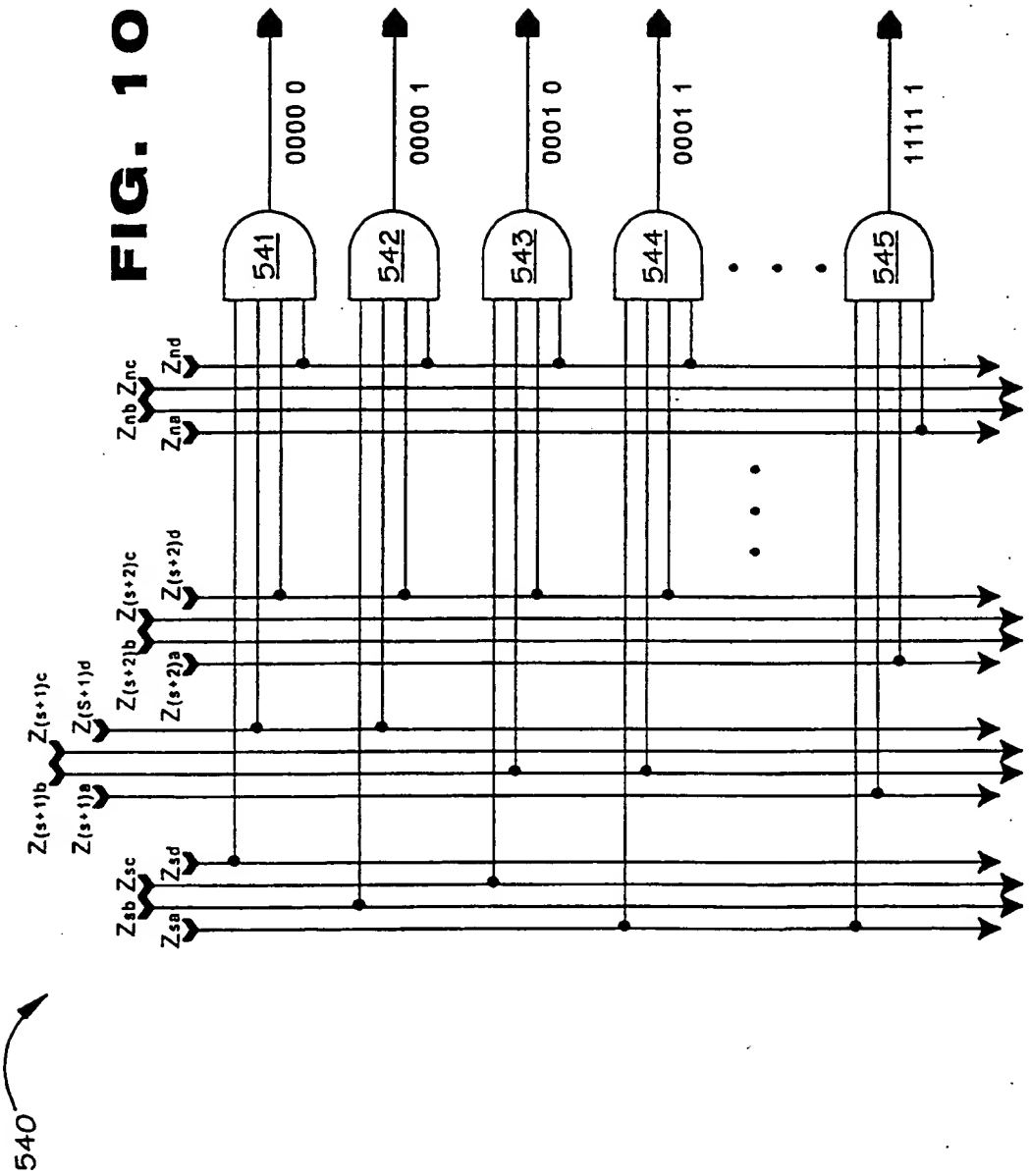

CACHE LINE 522
LOW BLOCK
526
HIGH BLOCK
524
520
CACHE
550
CACHE ENABLE LINES
REDUNDANT FORM DECODER
530
ADDRESS LINES
CACHE LINE DRIVER
540
ADDRESS DECODER
510
$\hat{S}_0$ $\hat{S}_1$ $\hat{S}_2$ $\hat{S}_3$ $\hat{S}_4$ $\hat{S}_5$ $\hat{S}_6$

FIG. 10


541
542
543
544
545
0000 0
0000 1
0001 0
0001 1
1111 1
Znd
Znc
Znb
Zna
Z(s+2)d
Z(s+2)c
Z(s+2)b
Z(s+2)a
Z(s+1)d
Z(s+1)c
Z(s+1)b
Z(s+1)a
Zsd
Zsc
Zsb
Zsa
540

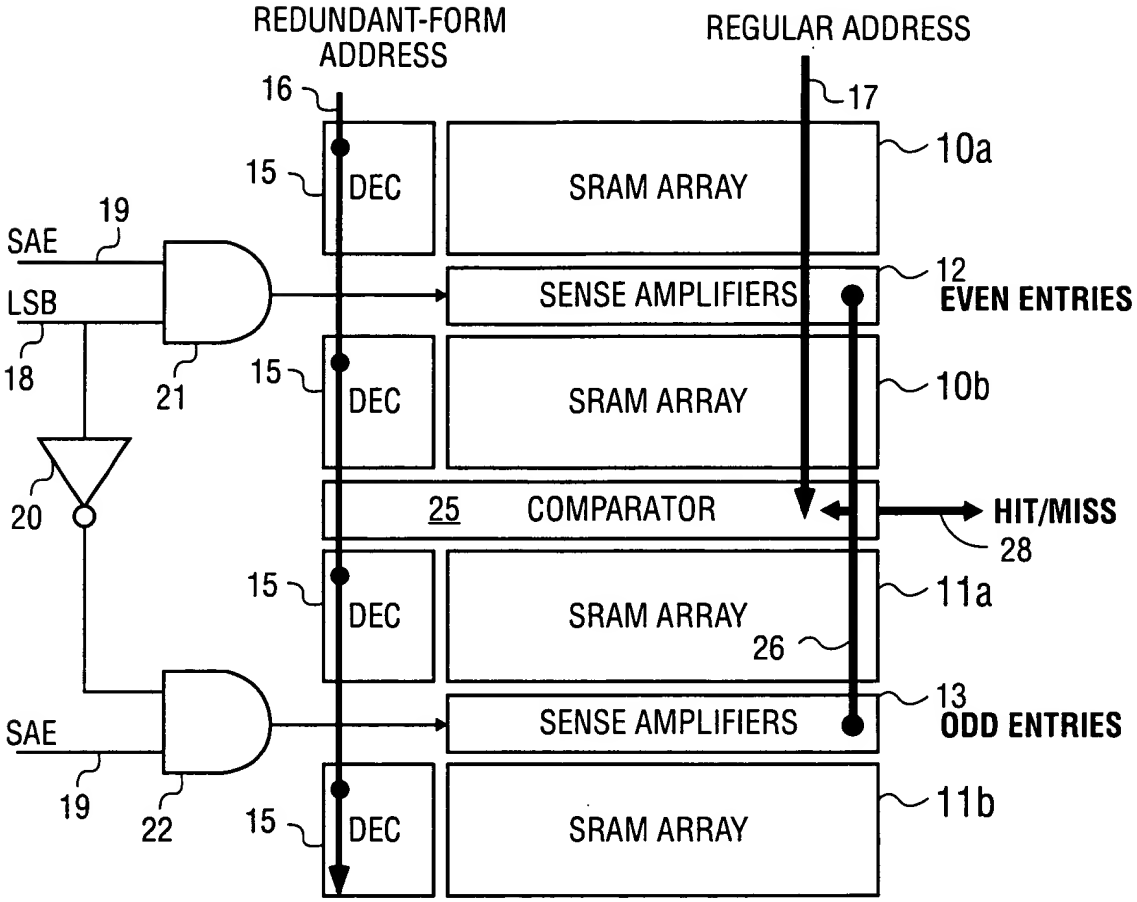

REDUNDANT-FORM ADDRESS
REGULAR ADDRESS
16
17
15
DEC
SRAM ARRAY
10a
19
SAE
LSB
18
21
SENSE AMPLIFIERS
12
EVEN ENTRIES
15
DEC
SRAM ARRAY
10b
20
25
COMPARATOR
HIT/MISS
28
15
DEC
SRAM ARRAY
11a
26
SAE
19
22
SENSE AMPLIFIERS
13
ODD ENTRIES
15
DEC
SRAM ARRAY
11b

FIG. 1

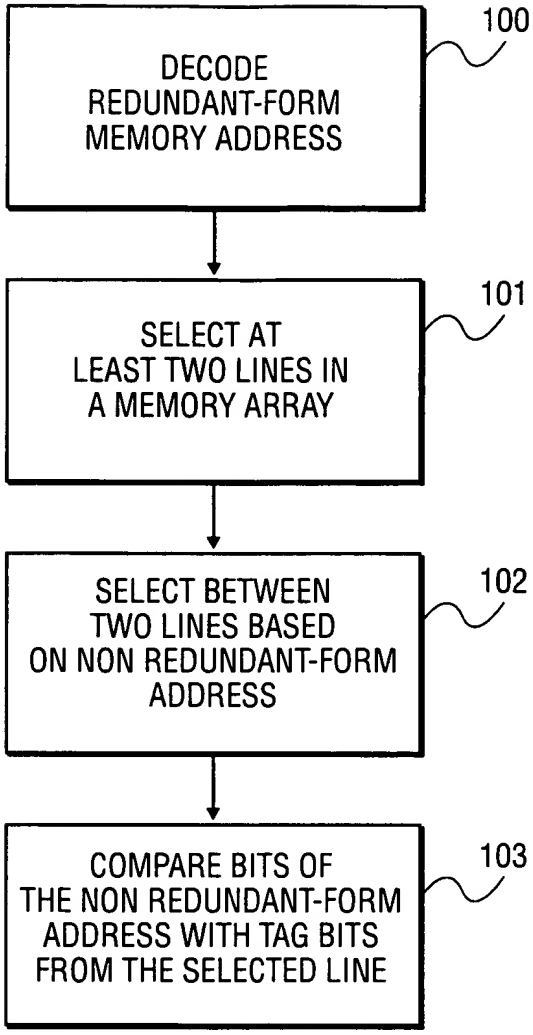

DECODE REDUNDANT-FORM MEMORY ADDRESS
100
SELECT AT LEAST TWO LINES IN A MEMORY ARRAY
101
SELECT BETWEEN TWO LINES BASED ON NON REDUNDANT-FORM ADDRESS
102
COMPARE BITS OF THE NON REDUNDANT-FORM ADDRESS WITH TAG BITS FROM THE SELECTED LINE
103

FIG. 2

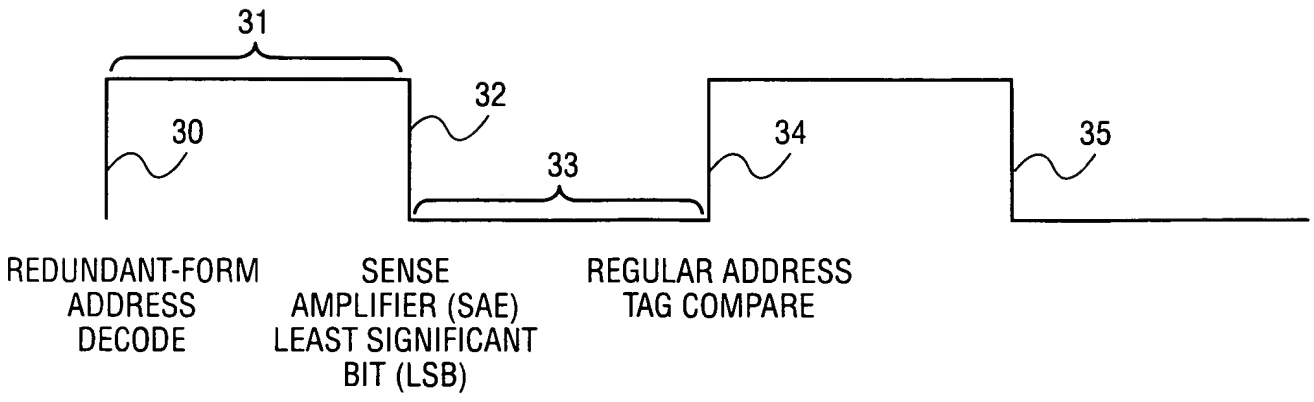

31
32
30
33
34
35
REDUNDANT-FORM ADDRESS DECODE
SENSE AMPLIFIER (SAE) LEAST SIGNIFICANT BIT (LSB)
REGULAR ADDRESS TAG COMPARE

FIG. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/12719

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : G06F 12/00, 9/34, 7/42; G11C 11/408, 11/418; HO3K 19/094
US CL : 711/3, 220; 365/230.06; 326/105; 708/670, 708

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 711/3, 104, 105, 118, 201, 219, 220; 708/493, 524, 670, 700, 706, 708; 365/230.06, 230.08; 326/105

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

US Automated Patent System (APS), files USPAT, JPOABS, EPOABS
search terms: redundant, form, decoder, add, adder, carry, save, propagate

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,754,819 A (LYNCH ET AL) 19 May 1998 (19.05.98), see column 1, lines 8-35; column 1, line 55 to column 2, line 5; and Figures 1, 3 and 6-8.	1-25
Y, P	US 5,815,420 A (STEISS) 29 September 1998 (29.09.98), see column 1, line 40 to column 2, line 27 and column 5, lines 31-45.	1-25
A	US 5,659,495 A (BRIGGS ET AL) 19 August 1997 (19.08.97), see column 2, lines 1-7 and column 5, lines 21-34.	1-25
A	US 5,467,318 A (MOTOMURA) 14 November 1995 (14.11.95), see entire document.	1-25
A	US 4,534,029 A (SINGH ET AL) 06 August 1985 (06.08.85), see entire document.	1-25

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
30 SEPTEMBER 1999	09NOV1999

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	GLENN GOSSAGE Joni Hill
Facsimile No. (703) 305-3230	Telephone No. (703) 305-3900

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/12719

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,625,582 A (TIMKO) 29 April 1997 (29.04.97), see entire document.	1-25
A	US 5,583,806 A (WIDIGEN ET AL) 10 December 1996 (10.12.96), see entire document.	1-25
A	Cortadella et al, "Evaluation of A + B = K Conditions Without Carry Propagation," IEEE Transactions on Computers, Volume 41, No. 11, November 1992, pp. 1484-1488.	1-25